

ふりがな 氏 名	みき たくじ 三木 拓司	職名	教授
部局 講座 教育研究分野名	科学技術イノベーション研究科 先端 IT 講座 先端 IT 分野	学位称号	博士（工学）
略歴（学歴，職歴，教育歴，所属機関，学会及び社会における活動，受賞）			
年 月	（学 歴）		
2000 年 3 月	京都市立紫野高等学校 卒業		
2000 年 4 月	立命館大学理工学部電気電子工学科 入学		
2004 年 3 月	同上 卒業		
2004 年 4 月	立命館大学大学院理工学研究科博士課程前期課程情報システム学専攻 入学		
2006 年 3 月	同上 修了		
2015 年 4 月	神戸大学大学院システム情報学研究科博士課程後期課程情報科学専攻 入学		
2017 年 3 月	同上 修了		
2017 年 3 月	博士（工学）（神戸大学）（博い第 974 号）		
年 月	（職 歴）		
2006 年 4 月	パナソニック株式会社 本社 R&D 部門 入社		
2010 年 4 月	パナソニック株式会社 R&D 本部 主任技師		
2017 年 3 月	パナソニック株式会社 退職		
2017 年 4 月	神戸大学大学院科学技術イノベーション研究科 特命准教授		
2022 年 6 月	神戸大学大学院科学技術イノベーション研究科 准教授（現在に至る）		
年 月	（受 賞）		
2011 年 5 月	電子情報通信学会 集積回路研究会 優秀若手講演賞		
2019 年 5 月	電子情報通信学会 集積回路研究会 2018年度若手研究会優秀ポスター賞		
2019 年 12 月	電子情報通信学会ハードウェアセキュリティ研究専門委員会若手優秀賞		
2020 年 11 月	キオクシア奨励研究2018 優秀研究賞		
2021 年 5 月	LSI とシステムのワークショップ 2021 IEEE SSCS Japan Chapter Academic Research Award		
2023 年 5 月	電子情報通信学会 集積回路研究会 優秀若手講演賞		

2023 年 5 月	LSI とシステムのワークショップ 2023 IEEE SSCS Japan Chapter Academic Research Award
2023 年 10 月	令和 5 年度 神戸大学学長表彰（財務貢献者）
2023 年 12 月	電子情報通信学会ハードウェアセキュリティ研究専門委員会若手優秀賞

教 育 研 究 上 の 業 績	
(著 書)	
1.	<u>三木拓司</u> センサーシステムを指向した AD 変換器の性能向上に関する研究 神戸大学博士論文，全 97 ページ，2017 http://www.lib.kobe-u.ac.jp/repository/thesis2/d1/D1006937.pdf
2.	<u>三木拓司</u> ，道正志郎 実践的 CMOS アナログ/RF 回路の設計法 科学情報出版株式会社，全 244 ページ，2020/11/28. (分担執筆) 全 11 章のうち 1,2,9,10,11 章を担当
3.	吉河武文， <u>三木拓司</u> 等価回路でしっかり理解！詳解 電子回路 オーム社，全 288 ページ，2021/8/27 (分担執筆) 全 15 章のうち 11,12,13,14,15 章，および演習問題を担当
(学 術 論 文)	
※ Web of Science に登録されている学術誌等に掲載されている論文等 (a. 学会誌，専門誌等に掲載された論文)	
1.	※ <u>Takuji Miki</u> , Takashi Morie, 他 2 名 An 11-b 300-MS/s Double-Sampling Pipelined ADC With On-Chip Digital Calibration for Memory Effects IEEE Journal of Solid-State Circuits, vol. 47, no. 11, pp. 2773-2782, Nov. 2012.
2.	※ <u>Takuji Miki</u> , Takashi Morie, 他 6 名 A 4.2 mW 50 MS/s 13 bit CMOS SAR ADC With SNR and SFDR Enhancement Techniques IEEE Journal of Solid-State Circuits, vol. 50, no. 6, pp. 1372-1381, Jun. 2015.
3.	※ Noriyuki Miura, Shiro Dosho, Hiroyuki Tezuka, <u>Takuji Miki</u> , 他 2 名 A 1 mm Pitch 80 x 80 Channel 322 Hz Frame-Rate Multitouch Distribution Sensor With Two-Step Dual-Mode Capacitance Scan IEEE Journal of Solid-State Circuits, vol. 50, no. 11, pp. 2741-2749, Nov. 2015.
4.	※ <u>Takuji Miki</u> , Noriyuki Miura, 他 3 名 A 500 MHz-BW -52.5 dB-THD Voltage-to-Time Converter Utilizing Two-Step Transition Inverter Delay Lines in 28nm CMOS IEICE Transactions on Electronics, Vol. E100-C, No. 6, pp. 560-567. Jun. 2017.

5. ※ Takuji Miki, Toshiaki Ozeki, Jun-ichi Naka
A 2GS/s 8-bit Time-Interleaved SAR ADC for Millimeter-Wave Pulsed Radar Baseband SoC
IEEE Journal of Solid-State Circuits, vol. 52, no. 10, pp. 2712-2720, Oct. 2017.
6. ※ Yuuki Araga, Makoto Nagata, Hiroaki Ikeda, Takuji Miki, 他 4 名
A Thick Cu Layer Buried in Si Interposer Backside for Global Power Routing
IEEE Transactions on Components, Packaging and Manufacturing Technology, Vol. 9, pp. 502-510, Mar. 2019.
7. ※ Takuji Miki, Noriyuki Miura, Makoto Nagata
A 0.72 pJ/bit 400um² Physical Random Number Generator Utilizing SAR Technique for Secure Implementation on Sensor Nodes
IEICE Transactions on Electronics, Vol. E102-C, No. 7, Jul. 2019.
8. ※ Takuji Miki, Noriyuki Miura, 他 3 名
A Random Interrupt Dithering SAR Technique for Secure ADC Against Reference-Charge Side-Channel Attack
IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 67, no. 1, Jan. 2020.
9. ※ Takuji Miki, Makoto Nagata, 他 7 名
Si-Backside Protection Circuits Against Physical Security Attacks on Flip-Chip Devices
IEEE Journal of Solid-State Circuits, vol. 55, no. 10, pp. 2747-2755, Oct. 2020.
10. ※ Takuya Wadatsumi, Takuji Miki, Makoto Nagata
A dual-mode successive approximation register analog to digital converter to detect malicious off-chip power noise measurement attacks
Japanese Journal of Applied Physics, vol. 60, no. SBBL03, pp.1-9, Feb. 2021.
11. ※ Kazuki Monta, Hiroki Sonoda, Takaaki Okidono, Yuuki Araga, Naoya Watanabe, Haruo Shimamoto, Katsuya Kikuchi, Noriyuki Miura, Takuji Miki, Makoto Nagata
3-D CMOS Chip Stacking for Security ICs Featuring Backside Buried Metal Power Delivery Networks With Distributed Capacitance
IEEE Transactions on Electron Devices, vol. 68, no. 4, pp. 2077-2082, Apr. 2021.
12. ※ Makoto Nagata, Takuji Miki, Noriyuki Miura
Physical Attack Protection Techniques for IC Chip Level Hardware Security
IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 30, no. 1, pp. 5-14, Jan. 2022.
13. ※ Hiroki Sonoda, Takuji Miki, Makoto Nagata
Measurement of Electromagnetic Field Immunity of Voltage-Controlled Oscillator-Based Analog-to-Digital Converters in 28 nm CMOS Technology
Japanese Journal of Applied Physics, Vol. 61, No. SC1045, pp.1-7, Feb. 2022.
14. ※ Takuji Miki, Makoto Nagata
Countermeasures against physical security attacks on ICs utilizing on-chip wideband ADCs
Japanese Journal of Applied Physics, vol. 61, no. SC0803, pp. 1-8, 2022.
15. ※ Takuji Miki, Ryoza Takahashi, Makoto Nagata
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for large-scale qubit arrays

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16. ※ Hiroki Sonoda, Ryo Kasai, Daisuke Tanaka, Yoshihide Murakami, Kyoshi Mihara, Yuuki Araga, Naoya Watanabe, Haruo Shimamoto, Katsuya Kikuchi, Takuji Miki, Makoto Nagata
In-Place Evaluation of Powering and Signaling Within Fan-Out Multiple IC Chip Packaging
IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 12, no. 7, pp. 1140-1149, Jul. 2022.
17. ※ Kazuki Monta, Leonidas Kataselas, Ferenc Fodor, Takuji Miki, Alkis Hatzopoulos, Makoto Nagata, Erik Jan Marinissen
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18. ※ Makoto Nagata, Noriyuki Miura, Takuji Miki
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IEEE Solid-State Circuits Magazine, vol. 15, no. 1, pp. 25-31, Jan. 2023.
19. ※ Ryozo Takahashi, Takuji Miki, Makoto Nagata
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20. ※ Takuya Wadatsumi, Kohei Kawai, Rikuu Hasegawa, Kikuo Muramatsu, Hiromu Hasegawa, Takuya Sawada, Takahito Fukushima, Hisashi Kondo, Takuji Miki, Makoto Nagata
Experimental Exploration of the Backside ESD Impacts on an IC Chip in Flip Chip Packaging
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21. 田口美里、高橋亮蔵、加藤薫子、楠野順弘、三木拓司、永田真
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電子情報通信学会論文誌 C, Vol. J107-C, No. 4, pp. 175-181, Apr. 2024.
22. ※ Tokio Futaya, Raisei Mizokuchi, Misato Taguchi, Takuji Miki, Makoto Nagata, Jun Yoneda, Tetsuo Kodaera
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23. ※ Takuya Wadatsumi, Kazuki Monta, Yusuke Hayashi, Takuji Miki, Alkis A. Hatzopoulos, Adrijan Barić, Makoto Nagata
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(b. 国際会議等の Proceedings に掲載された論文)

1. ※ Tsutomu Nishimura, Takuji Miki, 他 6 名
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2. ※ Kazuo Matsukawa, Takashi Morie, Yusuke Tokunaga, Shiro Sakiyama, Yosuke Mitani, Masao Takayama, Takuji Miki, 他 3 名
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3. ※ Takuji Miki, Takashi Morie, 他 2 名
An 11b 300MS/s 0.24pJ/conversion-step Double-Sampling Pipelined ADC with on-chip full digital calibration for all nonidealities including memory effects
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4. ※ Takashi Morie, Takuji Miki, 他 6 名
A 71dB-SNDR 50MS/s 4.2mW CMOS SAR ADC by SNR enhancement techniques utilizing noise
IEEE International Solid-State Circuits Conference Digest of Technical Papers, pp. 272-273, 2013.
5. ※ Noriyuki Miura, Shiro Dosho, Satoshi Takaya, Daisuke Fujimoto, Takuya Kiriya, Hiroyuki Tezuka, Takuji Miki, 他 2 名
A 1mm-Pitch 80x80-Channel 322Hz-Frame-Rate Touch Sensor with Two-Step Dual-Mode Capacitance Scan
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6. ※ Koji Obata, Kazuo Matsukawa, Takuji Miki, 他 2 名
A 97.99 dB SNDR, 2 kHz BW, 37.1 uW noise-shaping SAR ADC with dynamic element matching and modulation dither effect
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7. ※ Takuji Miki, Noriyuki Miura, 他 3 名
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8. ※ Takuji Miki, Toshiaki Ozeki, Jun-ichi Naka
A 2GS/s 8b Time-Interleaved SAR ADC for Millimeter-Wave Pulsed Radar Baseband SoC
Proceedings of IEEE Asian Solid-State Circuits Conference, pp. 5-8, 2016.
9. ※ Makoto Nagata, Takuji Miki, Noriyuki Miura
On-Chip Physical Attack Protection Circuits for Hardware Security
Proceedings of IEEE Custom Integrated Circuits Conference, pp. 1-6, 2019.
10. Takuji Miki, Makoto Nagata, 他 7 名
Over-the-top Si Interposer Embedding Backside Buried Metal PDN to Reduce Power Supply Impedance of Large Scale Digital ICs
Proceedings of IEEE 2019 International 3D Systems Integration Conference, pp.1-4, 2019.
11. ※ Takuji Miki, Makoto Nagata, 他 7 名
A Si-Backside Protection Circuits Against Physical Security Attacks on Flip-Chip Devices
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12. ※ Takuya Wadatsumi, Takuji Miki, Makoto Nagata
A Dual-mode SAR ADC Enabling On-chip Detection of Off-chip Power Noise Measurements by Attackers

- Proceedings of International Conference on Solid State Devices and Materials, pp. 789-790, 2020.
13. ※ Takuji Miki, Noriyuki Miura, 他 3 名
A Random Interrupt Dithering SAR Technique for Secure ADC Against Reference-Charge Side-Channel Attack
Proceedings of IEEE International Symposium on Circuits and Systems, 2020.
 14. ※ Hiroki Sonoda, Kazuki Monta, Takaaki Okidono, Yuuki Araga, Naoya Watanabe, Haruo Shimamoto, Katsuya Kikuchi, Noriyuki Miura, Takuji Miki, Makoto Nagata
Secure 3D CMOS Chip Stacks with Backside Buried Metal Power Delivery Networks for Distributed Decoupling Capacitance
Proceedings of IEEE International Electron Device Meeting, pp. 1-4, 2020.
 15. ※ Hiroki Sonoda, Takuji Miki, Makoto Nagata
Electromagnetic Susceptibility of VCO-based ADC in 28 nm CMOS Technology
Proceedings of International Conference on Solid State Devices and Materials, pp. 698-699, 2021.
 16. Koh Watanabe, Takuya Wadatsumi, Kazuki Monta, Mai Aoi, Misaki Komatsu, Ryota Sakai, Satoshi Tanaka, Takuji Miki, Makoto Nagata
Near Field Measurements of Sub-Millimeter-Wave Noise Emission from Digital Integrated Circuits
International Workshop on the Electromagnetic Compatibility of Integrated Circuits, pp. 45-47, Mar. 2022.
 17. ※ Takuya Wadatsumi, Kohei Kawai, Rikuu Hasegawa, Kikuo Muramatsu, Hiromu Hasegawa, Takuya Sawada, Takahito Fukushima, Hisashi Kondo, Takuji Miki, Makoto Nagata
Voltage Surges by Backside ESD Impacts on IC Chip in Flip Chip Packaging
Proceedings of IEEE International Reliability Physics Symposium (IRPS 2022), pp.1-6, Mar. 2022.
 18. ※ Noriyuki Miura, Kotaro Naruse, Jun Shiomi, Yoshihiro Midoh, Tetsuya Hirose, Takaaki Okidono, Takuji Miki, Makoto Nagata
A Triturated Sensing System
International Solid-State Circuits Conference (ISSCC), Digest of Technical Papers, pp. 216-217, Feb. 2023.
 19. ※ Takuya Wadatsumi, Kohei Kawai, Rikuu Hasegawa, Kazuki Monta, Takuji Miki, Makoto Nagata
Characterization of Backside ESD Impacts on Integrated Circuits
Proceedings of IEEE International Reliability Physics Symposium (IRPS 2023), P22, Mar. 2023.
 20. ※ Yuya Aoki, Tatsuya Iwata, Takuji Miki, Kazutoshi Kobayashi, Takefumi Yoshikawa
A 13-bit Radiation-Hardened SAR ADC with Error Correction by Adaptive Topology Transformation
Proceedings of IEEE International Reliability Physics Symposium (IRPS 2023), P22, Mar. 2023.
 21. ※ Kazuki Monta, Takumi Matsumaru, Takaaki Okidono, Takuji Miki, Makoto Nagata
Side-Channel Leakage Evaluation of Multi-Chip Cryptographic Modules
Workshop on Nano Security at DATE2023, Apr. 2023.
 22. ※ Takuya Wadatsumi, Rikuu Hasegawa, Kazuki Monta, Takaaki Okidono, Takuji Miki, Makoto Nagata
A Si-Interposer with Buried Cu Metal Stripes and Bonded to Si-Substrate Backside for Security IC Chips
Proceedings of the IEEE 73rd Electronic Components and Technology Conference (ECTC 2023), pp. 951-954, June 2023.

23. ※ Tokio Futaya, Raisei Mizokuchi, Misato Taguchi, Takuji Miki, Makoto Nagata, Jun Yoneda, Tetsuo Kodaera
Cryogenic Inter-chip Connection for Silicon Qubit Devices
Extended Abstracts of International Conference on Solid State Devices and Materials (SSDM), B-1-02, pp.69-70, Sep. 2023.
24. ※ Rikuu Hasegawa, Kazuki Monta, Takuya Wadatsumi, Takuji Miki and Makoto Nagata
On-chip evaluation of voltage drops and fault occurrence induced by Si backside EM injection
The 15th International Workshop on Constructive Side-Channel Analysis and Secure Design (COSADE2024), 2024.
25. ※ Misato Taguchi, Takaaki Okidono, Takuji Miki, Makoto Nagata
Si Interposer with Cu TSVs on Cu Substrate Thermally and Electrically Anchoring Qubit Chips in Millikelvin Assembly
IEEE 74th Electronic Components and Technology Conference (ECTC 2024), May 2024.
26. ※ Ryozo Takahashi, Yusuke Kanno, Takuji Miki, Nobuhiro Kusuno, Hiroyuki Mizuno, Makoto Nagata
A cryogenic pulse shaper for spin qubit control utilizing 1ns-time-resolution ADCs on an active silicon interposer operating at sub-100 mK temperatures
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(学 術 講 演)

1. Takuji Miki
Cryogenic Bias Voltage Control Circuits for Large Scale Qubit Arrays
28th Asia and South Pacific Design Automation Conference (ASP-DAC 2023) Designer's Forum, Jan. 18, 2023.
2. Takuji Miki
Cryogenic CMOS Analog Circuits toward Large-scale Silicon Quantum Computers
IEEE Asian Solid-State Circuits Conference (A-SSCC 2023), RiSE Forum, Nov. 2023.

(上記以外に 29 編)